REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
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PAGE	18	19	20	21	22	23															
REV STATUS OF PAGES	**REV**																				
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17		

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 13-01-17	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, 1.2 GHz CLOCK DISTRIBUTION IC, 1.6 GHz INPUTS, DIVIDERS, FIVE OUTPUTS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/12656**
	REV	**PAGE** 1 **OF** 23

AMSC N/A

5962-V041-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 1.2 GHz clock distribution IC, 1.6 GHz inputs, dividers, five outputs microcircuit, with an operating temperature range of -55°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12656	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD9512-EP	1.2 GHz clock distribution IC, 1.6 GHz inputs, dividers, five outputs

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	JEDEC MO-220-VKKD-2	Lead Frame Chip Scale Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

VS with respect to GND	-0.3 V to +3.6 V
DSYNC/DSYNCB with respect to GND	-0.3 V to V_S + 0.3 V
RSET with respect to GND	-0.3 V to V_S + 0.3 V
CLK1, CLK1B, CLK2, CLK2B with respect to GND	-0.3 V to V_S + 0.3 V
CLK1 with respect to CLK1B	-1.2 V to +1.2 V
CLK2 with respect to CLK2B	-1.2 V to +1.2 V
SCLK, SDIO, SDO, CSB with respect to GND	-0.3 V to V_S + 0.3 V
OUT0, OUT1, OUT2, OUT3, OUT4 with respect to GND	-0.3 V to V_S + 0.3 V
FUNCTION with respect to GND	-0.3 V to V_S + 0.3 V
SYNC STATUS with respect to GND	-0.3 V to V_S + 0.3 V
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
Lead temperature (10 sec)	300°C

1.4 Thermal characteristics.

Thermal resistance 2/

Case outline	θ_{JA}	Unit
Case X	28.5	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Thermal impedance measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 LVPECL differential output swing vs frequency. The LVPECL differential output swing vs frequency shall be as shown in figure 5.

3.5.6 LVDS differential output swing vs frequency. The LVDS differential output swing vs frequency shall be as shown in figure 6.

3.5.7 CMOS single ended output swing vs frequency and load. The CMOS single ended output swing vs frequency and load shall be as shown in figure 7.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
CLOCK INPUTS						
Clock inputs (CLK1, CLK2) 3/						
Input frequency			0		1.6	GHz
Input sensitivity		4/		150 7/		mV p-p
Input level		5/			2 8/	V p-p
Input common mode voltage	V_{CM}	6/	1.45	1.6	1.7	V
		At -40°C to +85°C	1.5	1.6	1.7	V
Input common mode range	V_{CMR}	With 200 mV p-p signal applied, dc-coupled	1.3		1.8	V
Input sensitivity, single ended		CLK2 ac-coupled; CLK2B ac bypassed to RF ground		150		mV p-p
Input resistance		Self-biased	4.0	4.8	5.6	kΩ
Input capacitance				2		pF
CLOCK OUTPUTS						
LVPECL clock outputs (Termination = 50 Ω to V_S – 2 V)						
OUT0, OUT1, OUT2; Differential		Output level 0x3D (0x3E) (0x3F)[3:2] = 10b				
Output frequency		See FIGURE 5			1200	MHz
Output high voltage	V_{OH}		V_S – 1.22	V_S – 0.98	V_S – 0.93	V
Output low voltage	V_{OL}		V_S – 2.10	V_S – 1.80	V_S – 1.67	V
Output differential voltage	V_{OD}		660	810	965	mV
LVDS clock outputs (Termination = 100 Ω differential; default)						
OUT3, OUT4; Differential		Output level 0x40 (0x41)[2:1] = 01b				
		3.5 mA termination current				
Output frequency		See FIGURE 6			800	MHz
Differential output voltage	V_{OD}		250	360	450	mV
Delta V_{OD}					25	mV
Output offset voltage	V_{OS}	At full temperature range	1.05	1.23	1.375	V
		At -40°C to +85°C	1.125	1.23	1.375	V
Delta V_{OS}					25	mV
Short Circuit current	I_{SA}, I_{SB}	Output shorted to GND		14	24	mA
CMOS clock outputs						
OUT3, OUT4		Single ended measurements;				
		B outputs: inverted, termination open				
Output frequency		With 5 pF load each outputs, see FIGURE 7			250	MHz
Output voltage high	V_{OH}	@ 1 mA load	V_S – 0.1			V
Output voltage low	V_{OL}	@ 1 mA load			0.1	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
TIMING CHARACTERISTICS						
LVPECL (Termination = 50 Ω to V_S – 2V, Output level 0x3D (0x3E)(0x3F)[3:2] =10b)						
Output rise time	t_{RP}	20% to 80%, measured differentially		130	180	ps
Output fall time	t_{FP}	80% to 20%, measured differentially		130	180	
Propagation delay, t_{PELC}, CLK-TO-LVPECL OUT 9/						
Divide = Bypass		At full temperature range	320	490	635	ps
		At -40°C to +85°C	335	490	635	
Divide = 2 to 32		At full temperature range	360	545	695	
		At -40°C to +85°C	375	545	695	
Variation with temperature				0.5		ps/°C
Output skew, LVPECL outputs						
OUT1 to OUT0 on same part 10/	t_{SKP}		70	100	140	ps
OUT1 to OUT2 on same part 10/	t_{SKP}		15	45	80	
OUT0 to OUT2 on same part 10/	t_{SKP}		45	65	90	
All LVPECL OUT across multiple parts 11/	t_{SKP_AB}				275	
Same LVPECL OUT across multiple parts 11/	t_{SKP_AB}				130	
LVDS (Termination = 100 Ω differential, Output level 0x40 (0x41)[2:1] = 01b, 3.5 mA termination current)						
Output rise time	t_{RL}	20% to 80%, measured differentially		200	350	ps
Output fall time	t_{FL}	80% to 20%, measured differentially		210	350	
Propagation delay, t_{LVDS}, CLK-to-LVDS OUT 9/ **OUT3 to OUT4**						
Divide = Bypass		At full temperature range	0.97	1.33	1.59	ns
		At -40°C to +85°C	0.99	1.33	1.59	
Divide = 2 to 32		At full temperature range	1.02	1.38	1.64	
		At -40°C to +85°C	1.04	1.38	1.64	
Variation with temperature				0.9		ps/°C
Output skew, LVDS outputs						
OUT3 to OUT4 on same part, 10/	t_{SKV}		-85		+270	ps
All LVDS OUTs across multiple parts 11/	t_{SKV_AB}				450	
Same LVDS OUT across multiple parts 11/	t_{SKV_AB}				325	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
TIMING CHARACTERISTICS-Continued.						
CMOS (B outputs are inverted; termination = open)						
Output rise time	t_{RC}	20% to 80%, C_{LOAD} = 3 pF		681	865	ps
Output fall time	t_{FC}	80% to 20%, C_{LOAD} = 3 pF		646	992	
Propagation delay, t_{CMOS}, CLK to CMOS OUT 9/						
Divide = Bypass		At full temperature range	1.0	1.39	1.71	ns
		At -40°C to +85°C	1.02	1.39	1.71	
Divide = 2 to 32		At full temperature range	1.05	1.44	1.76	
		At -40°C to +85°C	1.07	1.44	1.76	
Variation with temperature				1		ps/°C
Output skew, CMOS outputs						
OUT3 to OUT4 on same part, 10/	t_{SKC}		-140	+145	+300	ps
All CMOS OUT across multiple parts 11/	t_{SKC_AB}				650	
Same CMOS OUT across multiple parts 11/	t_{SKC_AB}				500	
LVPECL to LVDS OUT (Everything the same; different logic type LVPECL to LVDS on same part)						
Output skew	t_{SKP_V}		0.73	0.92	1.14	ns
LVPECL to CMOS OUT (Everything the same; different logic type LVPECL to CMOS on same part)						
Output skew	t_{SKP_C}		0.87	1.14	1.43	ns
LVDS to CMOS OUT (Everything the same; different logic type LVDS to CMOS on same part)						
Output skew	t_{SKV_C}		158	353	506	ps

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
CLOCK OUTPUT PHASE NOISE						
CLK1 to LVPECL and additive phase noise						
CLK1 = 622.08 MHz, OUT = 622.08 MHz		Input slew rate > 1 V/ns				
Divide Ratio = 1						
@ 10 Hz Offset				-125		dBc/Hz
@ 100 Hz Offset				-132		
@ 1 kHz Offset				-140		
@ 10 KHz Offset				-148		
@100 kHz Offset				-153		
> 1 MHz Offset				-154		
CLK1 = 622.08 MHz, OUT = 155.52 MHz						
Divide Ratio = 4						
@ 10 Hz Offset				-128		dBc/Hz
@ 100 Hz Offset				-140		
@ 1 kHz Offset				-148		
@ 10 KHz Offset				-155		
@100 kHz Offset				-161		
> 1 MHz Offset				-161		
CLK1 = 622.08 MHz, OUT = 38.88 MHz						
Divide Ratio = 16						
@ 10 Hz Offset				-135		dBc/Hz
@ 100 Hz Offset				-145		
@ 1 kHz Offset				-158		
@ 10 KHz Offset				-165		
@100 kHz Offset				-165		
> 1 MHz Offset				-166		
CLK1 = 491.52 MHz, OUT = 61.44 MHz						
Divide Ratio = 8						
@ 10 Hz Offset				-131		dBc/Hz
@ 100 Hz Offset				-142		
@ 1 kHz Offset				-153		
@ 10 KHz Offset				-160		
@100 kHz Offset				-165		
> 1 MHz Offset				-165		
CLK1 = 491.52 MHz, OUT = 245.76 MHz						
Divide Ratio = 2						
@ 10 Hz Offset				-125		dBc/Hz
@ 100 Hz Offset				-132		
@ 1 kHz Offset				-140		
@ 10 KHz Offset				-151		
@100 kHz Offset				-157		
> 1 MHz Offset				-158		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
CLOCK OUTPUT PHASE NOISE- Continued.						
CLK1 to LVPECL and additive phase noise – Continued.						
CLK1 = 245.76 MHz, OUT = 61.44 MHz						
Divide Ratio = 4						
@ 10 Hz Offset				-138		dBC/Hz
@ 100 Hz Offset				-144		
@ 1 kHz Offset				-154		
@ 10 KHz Offset				-163		
@100 kHz Offset				-164		
> 1 MHz Offset				-165		
CLK1 to LVDS additive phase noise						
CLK1 = 622.08 MHz, OUT = 622.08 MHz						
Divide Ratio = 1						
@ 10 Hz Offset				-100		dBC/Hz
@ 100 Hz Offset				-110		
@ 1 kHz Offset				-118		
@ 10 KHz Offset				-129		
@100 kHz Offset				-135		
@1 MHz Offset				-140		
> 10 MHz Offset				-148		
CLK1 = 622.08 MHz, OUT = 155.52 MHz						
Divide Ratio = 4						
@ 10 Hz Offset				-112		dBC/Hz
@ 100 Hz Offset				-122		
@ 1 kHz Offset				-132		
@ 10 KHz Offset				-142		
@100 kHz Offset				-148		
@1 MHz Offset				-152		
> 10 MHz Offset				-155		
CLK1 = 491.52 MHz, OUT = 245.76 MHz						
Divide Ratio = 2						
@ 10 Hz Offset				-108		dBC/Hz
@ 100 Hz Offset				-118		
@ 1 kHz Offset				-128		
@ 10 KHz Offset				-138		
@100 kHz Offset				-145		
@1 MHz Offset				-148		
> 10 MHz Offset				-154		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
CLOCK OUTPUT PHASE NOISE- Continued.						
CLK1 to LVDS additive phase noise – Continued.						
CLK1 = 491.52 MHz, OUT = 122.88 MHz						
Divide Ratio = 4						
@ 10 Hz Offset				-118		dBC/Hz
@ 100 Hz Offset				-129		
@ 1 kHz Offset				-136		
@ 10 KHz Offset				-147		
@100 kHz Offset				-153		
@1 MHz Offset				-156		
> 10 MHz Offset				-158		
CLK1 = 245.76 MHz, OUT = 245.76 MHz						
Divide Ratio = 1						
@ 10 Hz Offset				-108		dBC/Hz
@ 100 Hz Offset				-118		
@ 1 kHz Offset				-128		
@ 10 KHz Offset				-138		
@100 kHz Offset				-145		
@1 MHz Offset				-148		
> 10 MHz Offset				-155		
CLK1 = 245.76 MHz, OUT = 122.88 MHz						
Divide Ratio = 2						
@ 10 Hz Offset				-118		dBC/Hz
@ 100 Hz Offset				-127		
@ 1 kHz Offset				-137		
@ 10 KHz Offset				-147		
@100 kHz Offset				-154		
@1 MHz Offset				-156		
> 10 MHz Offset				-158		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
CLOCK OUTPUT PHASE NOISE- Continued.						
CLK1 to CMOS additive phase noise						
CLK1 = 245.76 MHz, OUT = 245.76 MHz						
Divide Ratio = 1						
@ 10 Hz Offset				-110		dBC/Hz
@ 100 Hz Offset				-121		
@ 1 kHz Offset				-130		
@ 10 KHz Offset				-140		
@100 kHz Offset				-145		
@1 MHz Offset				-149		
> 10 MHz Offset				-156		
CLK1 = 245.76 MHz, OUT = 61.44 MHz						
Divide Ratio = 4						
@ 10 Hz Offset				-122		dBC/Hz
@ 100 Hz Offset				-132		
@ 1 kHz Offset				-143		
@ 10 KHz Offset				-152		
@100 kHz Offset				-158		
@1 MHz Offset				-160		
> 10 MHz Offset				-162		
CLK1 = 78.6432 MHz, OUT = 78.6432 MHz						
Divide Ratio = 1						
@ 10 Hz Offset				-122		dBC/Hz
@ 100 Hz Offset				-132		
@ 1 kHz Offset				-140		
@ 10 KHz Offset				-150		
@100 kHz Offset				-155		
@1 MHz Offset				-158		
> 10 MHz Offset				-160		
CLK1 = 78.6432 MHz, OUT = 39.3216 MHz						
Divide Ratio = 2						
@ 10 Hz Offset				-128		dBC/Hz
@ 100 Hz Offset				-136		
@ 1 kHz Offset				-146		
@ 10 KHz Offset				-155		
@100 kHz Offset				-161		
> 1 MHz Offset				-162		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
CLOCK OUTPUT PHASE NOISE- Continued.					
LVPECL output additive time jitter					
CLK1 = 622.08 MHz Any LVPECL (OUT0 to OUT2) = 622.08 MHz, Divide ratio = 1	BW = 12 kHz to 20 MHz (OC-12)		40		fs rms
CLK1 = 622.08 MHz Any LVPECL (OUT0 to OUT2) = 155.52 MHz, Divide ratio = 4	BW = 12 kHz to 20 MHz (OC-3)		55		fs rms
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz, Divide ratio = 4	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz		215		fs rms
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz, Divide ratio = 4 Other LVPECL = 100 MHz Both LVDS (OUT3, OUT4) = 100 MHz	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		215		fs rms
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz, Divide ratio = 4 Other LVPECL = 50 MHz Both LVDS (OUT3, OUT4) = 50 MHz	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		222		fs rms
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz, Divide ratio = 4 Other LVPECL = 50 MHz Both CMOS (OUT3, OUT4) = 50 MHz (B outputs Off)	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		225		fs rms
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz, Divide ratio = 4 Other LVPECL = 50 MHz Both CMOS (OUT3, OUT4) = 50 MHz (B outputs On)	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		225		fs rms

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
CLOCK OUTPUT PHASE NOISE- Continued.					
LVDS output additive time jitter					
CLK1 = 400 MHz LVDS (OUT3) = 100 MHz Divide ratio = 4	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz		264		fs rms
CLK1 = 400 MHz LVDS (OUT4) = 100 MHz Divide ratio = 4	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz		319		fs rms
CLK1 = 400 MHz LVDS (OUT3) = 100 MHz Divide ratio = 4 LVDS (OUT4) = 50 MHz All LVPECL = 50 MHz	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		395		fs rms
CLK1 = 400 MHz LVDS (OUT4) = 100 MHz Divide ratio = 4 LVDS (OUT3) = 50 MHz All LVPECL = 50 MHz	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		395		fs rms
CLK1 = 400 MHz LVDS (OUT3) = 100 MHz Divide ratio = 4 CMOS (OUT4) = 50 MHz (B Outputs Off) All LVPECL = 50 MHz	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		367		fs rms
CLK1 = 400 MHz LVDS (OUT4) = 100 MHz Divide ratio = 4 CMOS (OUT3) = 50 MHz (B Outputs Off) All LVPECL = 50 MHz	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		367		fs rms
CLK1 = 400 MHz LVDS (OUT3) = 100 MHz Divide ratio = 4 CMOS (OUT4) = 50 MHz (B Outputs On) All LVPECL = 50 MHz	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		548		fs rms

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Test conditions 2/	Limits			Unit
		Min	Typ	Max	
CLOCK OUTPUT PHASE NOISE- Continued.					
LVDS output additive time jitter – Continued.					
CLK1 = 400 MHz LVDS (OUT4) = 100 MHz Divide ratio = 4 CMOS (OUT3) = 50 MHz (B Outputs On) All LVPECL = 50 MHz	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		548		fs rms
CMOS output additive time jitter					
CLK1 = 400 MHz Both CMOS (OUT3, OUT4) = 100 MHz (B output On) Divide ratio = 4	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz		275		
CLK1 = 400 MHz CMOS (OUT3) = 100 MHz (B output On) Divide ratio = 4 All LVPECL = 50 MHz LVDS (OUT4) = 50 MHz	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		400		
CLK1 = 400 MHz CMOS (OUT3) = 100 MHz (B output On) Divide ratio = 4 All LVPECL = 50 MHz CMOS (OUT4) = 50 MHz (B output Off)	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		374		
CLK1 = 400 MHz CMOS (OUT3) = 100 MHz (B output On) Divide ratio = 4 All LVPECL = 50 MHz CMOS (OUT4) = 50 MHz (B output On)	Calculated from SNR of ADC method; fc = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)		555		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
SERIAL CONTROL PORT						
CSB, SCLK (Inputs) 12/						
Input logic 1 voltage			2.0			V
Input logic 0 voltage					0.8	
Input logic 1 current				110		µA
Input logic 0 current					1	
Input capacitance				2		pF
SDIO (when input)						
Input logic 1 voltage			2.0			V
Input logic 0 voltage					0.8	
Input logic 1 current				10		nA
Input logic 0 current				10		
Input capacitance				2		pF
SDIO, SDO (Outputs)						
Input logic 1 voltage			2.7			V
Input logic 0 voltage					0.4	
Timing						
Clock rate (SCLK, $1/t_{SCLK}$)					25	MHz
Pulse width high	t_{PWH}		16			ns
Pulse width low	t_{PWL}		16			
SDIO to SCLK setup	t_{DS}		2			
SCLK to SDIO hold	t_{DH}		1			
SCLK to valid SDIO and SDO	t_{DV}		6			
CSB to SCLK setup and hold	t_S, t_H		2			
CSB minimum pulse width high	t_{PWH}		3			
FUNCTION PIN						
Input characteristics 13/						
Input logic 1 voltage			2.0			V
Input logic 0 voltage					0.8	
Input logic 1 current				110		µA
Input logic 0 current					1	
Capacitance				2		pF
Reset timing						
Pulse width low			50			ns
SYNC timing						
Pulse width low		14/	1.5			High speed clock cycles

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
SYNC STATUS PIN						
Output characteristics						
Output voltage high	V_{OH}		2.7			V
Output voltage low	V_{OL}				0.4	
POWER						
Power up default mode power dissipation		15/		550	600	mW
Power dissipation		16/			800	mW
		17/			850	
Full sleep power down		18/		35	60	
Power down (PDB)		19/		60	80	
Power delta						
CLK1, CLK2 power down			10	15	25	mW
Divider, DIV 2 to 32 bypass		For each divider.	23	27	33	
LVPELL output power down (PD2, PD3)		For each output. Does not include dissipation in termination (PD2 only)	50	65	75	
LVDS Output power down		For each output	80	92	110	
CMOS output power down (Static)		For each output. Static (no clock)	56	70	85	
CMOS output power down (Dynamic)		For each CMOS output, single ended. Clocking at 62 MHz with 5 pF load.	115	150	190	
CMOS output power down (Dynamic)		For each CMOS output, single ended. Clocking at 125 MHz with 5 pF load.	125	165	210	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Typical (Typ) is given for V_S = 3.3 V ±5%; T_A = 25°C, R_{SET} = 4.12 kΩ, unless otherwise noted. Minimum (Min) and Maximum (Max) values are given over full V_S and T_A (-55°C to +85°C) variation.
3/ CLK1 and CLK2 are electrically identical; each can be used as either differential or single ended input.
4/ Jitter performance can be improved with high slew rates (greater swing).
5/ Larger swing turn on protection diodes and can degrade jitter performance.
6/ Self biased; enables ac coupling; at full temperature range.
7/ With a 50 Ω termination, this is -12.5 dBm.
8/ With a 50 Ω termination, this is +10 dBm.
9/ The measurements are for CLK1. For CLK2, add approximately 25 ps.
10/ This is the difference between any two similar delay paths within a single device operating at the same voltage and temperature.
11/ This is the difference between any two similar delay paths across multiple devices operating at the same voltage and temperature
12/ CSB and SCLK have 30 kΩ internal pull down resistor.
13/ The FUNCTION pin has a 30 kΩ internal pull down resistor. This pin should normally be held high. Do not let input float.
14/ High speed clock is CLK1 or CLK2, whichever is being used for distribution.
15/ Power up default state; does not include power dissipated in output load resistors. No clock.
16/ All outputs on. Three LVPECL outputs @ 800 MHz, two CMOS out @ 62 MHz (5 pF load). Does not include power dissipated in external resistors.
17/ All outputs on. Three LVPECL outputs @ 800 MHz, two CMOS out @ 125 MHz (5 pF load). Does not include power dissipated in external resistors.
18/ Maximum sleep is entered by setting 0x0A[1:0] = 01b and 0x58[4] = 1b. This power off all band gap references. Does not include power dissipated in terminations.
19/ Set FUNCTION pin for PDB operation by setting 0x58[6:5] = 11b. Pull PDB low. Does not include power dissipated in terminations.

Case X

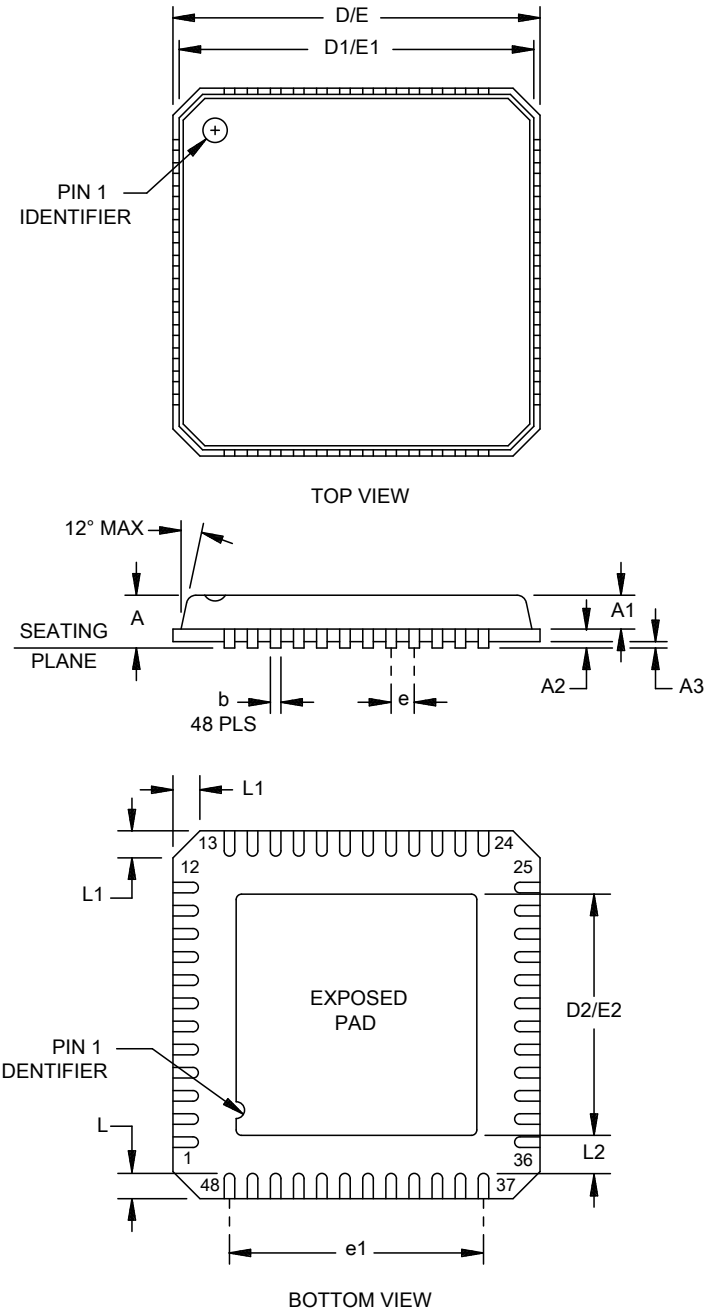

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12656
		REV	PAGE 18

Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	D2/E2	4.95	5.25
A1		0.80	e	0.50 BSC	
A2	0.20 REF		e1	5.50 REF	
A3		0.05	L	0.30	0.50
b	0.18	0.30	L1		0.60
D/E	7.00 BSC		L2	0.25	
D1/E1	6.75 BSC				

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-220-VKKD-2.

FIGURE 1. Case outline - Continued.

Case outline X							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DSYNC	13	SYNC STATUS	25	VS	37	GND
2	DSYNCB	14	SCLK	26	OUT1B	38	GND
3	VS	15	SDIO	27	OUT1	39	VS
4	VS	16	SDO	28	VS	40	VS
5	DNC	17	CSB	29	VS	41	OUT0B
6	VS	18	VS	30	OUT4B	42	OUT0
7	CLK2	19	GND	31	OUT4	43	GND
8	CLK2B	20	OUT2B	32	VS	44	VS
9	VS	21	OUT2	33	VS	45	RSET
10	CLK1	22	VS	34	OUT3B	46	GND
11	CLK1B	23	VS	35	OUT3	47	VS
12	FUNCTION	24	GND	36	VS	48	VS

FIGURE 2. Terminal connections.

Case outline X		
Terminal number	**Mnemonic**	**Description**
1	DSYNC	Detect Sync. Use for multichip synchronization.
2	DSYNCB	Detect Sync. Complement. Used for multichip synchronization.
3, 4, 6, 9, 18, 22, 23, 25, 28, 29, 32, 33, 36, 39, 40 44, 47, 48	VS	Power supply (3.3 V).
5	DNC	Do Not Connect. Do not connect to this pin.
7	CLK2	Clock input.
8	CLK2B	Complementary Clock input. Used in conjunction with CLK2.
10	CLK1	Clock input.
11	CLK1B	Complementary Clock input. Used in conjunction with CLK1.
12	FUNCTION	Multipurpose Input. Can be programmed as a reset (RESETB), sync (SYNCB), or power down (PDB) pin.
13	SYNC STATUS	Output Used to Monitor the Status of Multichip Synchronization.
14	SCLK	Serial Data Clock.
15	SDIO	Serial Data I/O.
16	SDO	Serial Data Output.
17	CSB	Serial Port Chip Select.
19, 24, 37, 38, 43, 46	GND	Ground.
20	OUT2B	Complementary LVPECL Output.
21	OUT2	LVPECL Output.
26	OUT1B	Complementary LVPECL Output.
27	OUT1	LVPECL Output.
30	OUT4B	Complementary LVDS/Inverted CMOS Output.
31	OUT4	LVDS/CMOS Output.
34	OUT3B	Complementary LVDS/Inverted CMOS Output.
35	OUT3	LVDS/CMOS Output.
41	OUT0B	Complementary LVPECL Output.
42	OUT0	LVPECL Output.
45	RSET	Current Set Resistor to Ground. Nominal value = 4.12 kΩ.
	EPAD	Exposed paddle. The exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground, GND.

FIGURE 3. Terminal function.

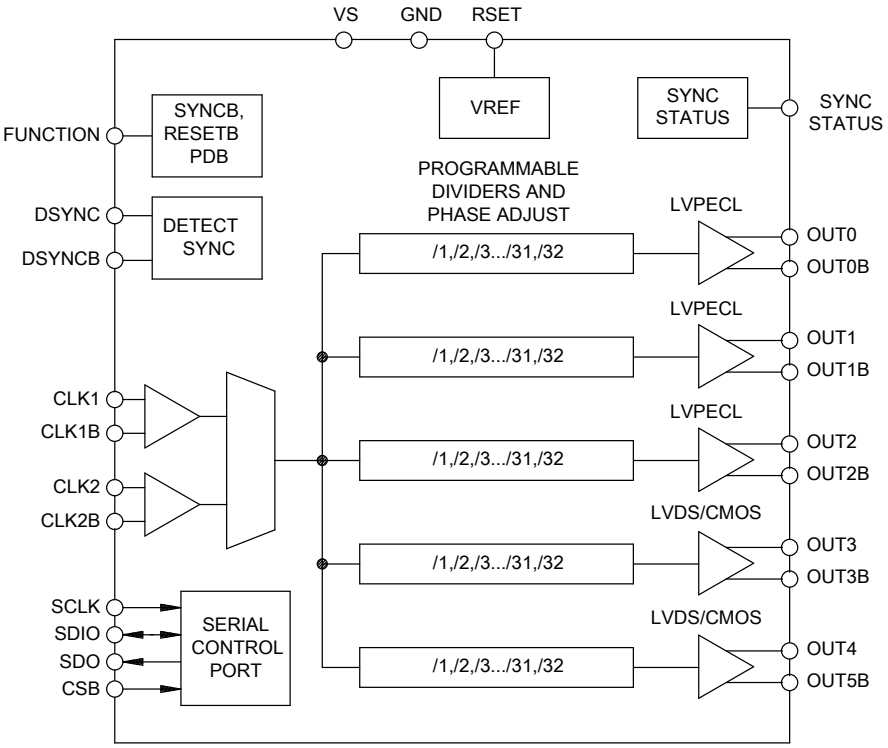

FIGURE 4. Functional block diagram.

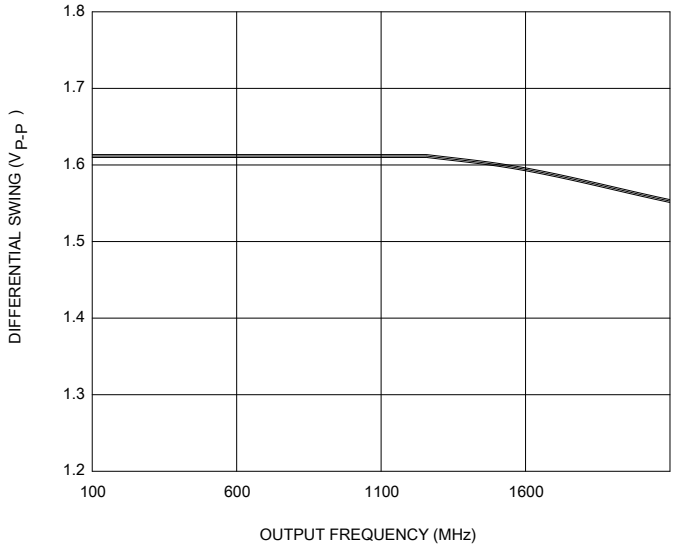

FIGURE 5. LVPECL differential output swing vs frequency.

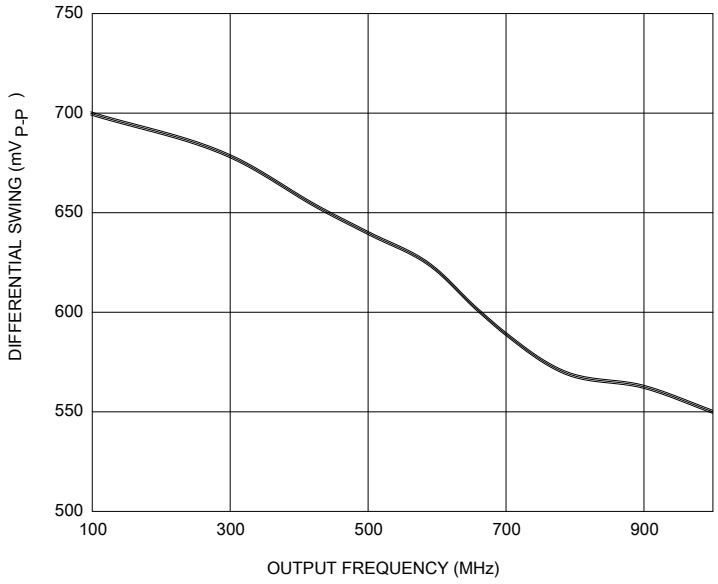

FIGURE 6. LVDS differential output swing vs frequency.

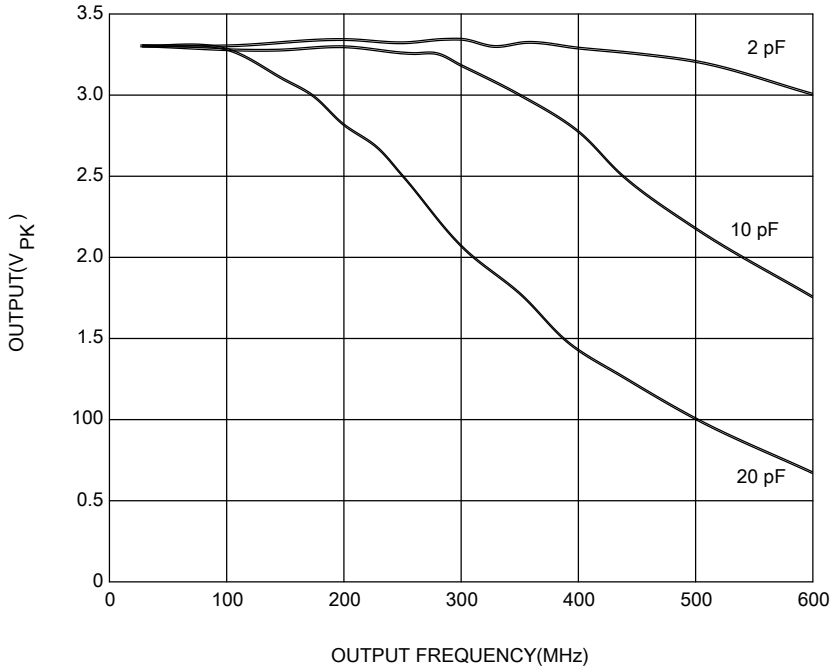

FIGURE 7. CMOS single ended output swing vs frequency and load.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12656-01XE	24355	AD9512UCPZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106